PROCESS FOR FORMING DUAL METAL GATE STRUCTURES

Abstract of the Disclosure

A semiconductor device has a P channel gate stack comprising a first metal type and a second metal type over the first metal type and an N channel gate stack comprising the second metal type in direct contact with a gate dielectric / etch stop layer stack. The N channel gate stack and the P channel gate stack are etched by a dry etch. Either the gate dielectric or etch stop can be in contact with the substrate. The etch stop layer prevents the dry etch of the first and second metal layers from etching through the gate dielectric and gouging the underlying substrate.